REMARKS

In this Response, Claims 1 and 8 are amended, Claim 3 is canceled, and Claims 9 and 10 are added. Claims 1 and 3-9 remain in the Application. Reconsideration of the pending claims is respectfully requested in view of the above amendment and the following remarks.

I. Claims Rejected Under 35 U.S.C. § 103(a)

Claim 1 and 4-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6.522.200 issued to Siniscalchi ("Siniscalchi").

Claim 1 is amended to incorporate all the limitations of the allowable Claim 3. Thus, for the same reasons that Claim 3 is allowable, amended Claim 1 is also allowable.

Claims 4-7 depend from Claim 1 and incorporate the limitations thereof. Thus, for at least the reasons mentioned above in regard to Claim 1, Siniscalchi does not teach or suggest these dependent claims. Accordingly, reconsideration and withdrawal of the § 103 rejection of Claims 1 and 4-7 are respectfully requested.

New Claims 9 and 10

New Claim 9 incorporates all of the limitations of Claims 1 and 2 as originally filed, and additionally includes the feature of "the second input voltage being different from the first input voltage." New Claim 10 depends from Claim 9 and further includes the features recited in Claim 5. The variable gain amplifier recited in Claims 9 and 10 correspond to the embodiment shown in FIG. 2 of Applicants' specification.

Siniscalchi does disclose the variable gain amplifier recited in Claims 9 and 10.

Siniscalchi implements a process-insensitive, highly linear, constant transconductance circuit, which compensates for variation in circuit operations caused by resistor processing variations. The transconductance circuit includes an offset biased CMOS multiplier to compensate for transconductance variations due to resistor processing variations. The transconductance value of the offset biased multiplier is kept constant.

The input stage of Siniscalchi includes amplifiers A1 and A2, transistors M11 and M12, current sources 404 and 406, and a resistor R (FIG. 4). The input stage of Siniscalchi does not teach the voltage-current converter (V-I converter) of the claimed invention.

Siniscalchi's circuit is configured to have a stabilized DC bias by means of the amplifiers A1 and A2 and to obtain wideband characteristics according to resistor R (FIG. 4 of Siniscalchi). The configuration of Siniscalchi's circuit is similar to that of an input stage of a folded-cascode OP-amplifier, which is a well-known circuit configuration. In addition, Siniscalchi's circuit and transistors M3-M6 and M7-M10 have a cascode configuration, and thus, cannot achieve low voltage operation.

By contrast, the V-I converter of the claimed invention may be implemented as resistors R21 and R22 (as in Claim 9) or a source follower circuit (as in Claim 1) having first and second NMOS transistors and current sources in order to accomplish a wide range of an input signal that guarantees linearity within a low voltage range. The current source of the input stage (the source follower circuit) is separately disposed from a current source of the output stage (the voltage-current converter circuit) for low voltage operation.

Therefore, the circuit configuration and purpose of the claimed invention are different from those of Siniscalchi.

The claimed invention is a complementary metal oxide semiconductor (CMOS) circuit having an operating frequency range of over 100MHz. Due to limitations in reduction of the threshold voltage in the MOS device, the input/output signal voltage is limited. It is thus difficult to expect smooth circuit operation for a low power supply. To overcome these problems, the claimed invention provides an integrated circuit (IC) embedded type CMOS variable gain amplifier having low power consumption characteristics and achieving high-speed operation at a low voltage in an integrated circuit. The CMOS variable gain amplifier has the following characteristics:

1) Operative at a low voltage;

2) Capable of processing an input signal having a wide range;

3) Performs variable gain amplification; and

4) Exhibits low distortion and high frequency bandwidth/wideband operating characteristics due to a stabilized current bias.

Thus, the claimed invention has many advantages over the prior art devices.

With respect to Claim 10, Claim 10 depends from Claim 9 and incorporates the limitations thereof. Thus, for at least the reasons mentioned above in regard to Claim 9, Siniscalchi does not teach or suggest each of the elements of Claim 10.

Moreover, Siniscalchi's transistors M9 to M10 and transistors M7 to M10 do not teach or suggest the current-voltage converter (I-V converter) of Claim 10.

The claimed current-voltage converter includes resistors R23 and R24 or active loads 41 and 42, NMOS transistors N25 and N26 driven by an external bias voltage Vb1, and current sources Is1 and Is2 driven by another external bias voltage Vb1. The function and purpose of the claimed current-voltage converter are different from those of Siniscalchi. Specifically, Siniscalchi is directed to the analog multiplier having the input stage of the folded-cascode amplifier, which is well known in the field. In the claimed invention, the input stage (the V-I converter) and the output stage (the I-V converter) share the current shared circuit using a separate DC bias to avoid voltage stacking, and, therefore, low voltage operation is achieved. Meanwhile, the configuration of Siniscalchi's circuit includes voltage stacking, and thus low voltage operation cannot be achieved.

Thus, Siniscalchi does not teach or suggest each of the elements of Claims 9 and 10. Accordingly, allowance of Claims 9 and 10 are respectfully requested.

II. Allowable Subject Matter

Applicants appreciate the Examiner's indication that Claims 3 and 8 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. Claim 3 is canceled and Claim 8 is amended to include all of the limitations of Claims 1 and 6. Thus, Claim 8 is in condition for allowance. Accordingly, reconsideration and withdrawal of the objection of Claims 3 and 8 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Amber D. Saunders 10/18/06

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